WHAT IS CLAIMED IS:

1. A random access memory (RAM) comprising:

a command block configured to provide a row signal having an active state in response to receiving a write command, wherein the active state occurs at a set time after receipt of the write command, and configured to provide a write signal having at least a first active state, wherein the first active state of the write signal occurs at a set delay after the active state of the row signal; and

an array of memory cells arranged in a plurality of rows and columns, wherein a selected row is opened for access in response to the active state of the row signal, and wherein data is written to at least one memory cell in the opened row in response to the at least first active state of the write signal.

2. The RAM of claim 1, further comprising a refresh block configured to perform autonomous refresh operations of memory cells of the array to maintain a proper status of the data stored therein, wherein the refresh block and the array are configured to perform a refresh operation at least within the set time, and wherein the refresh block is configured to provide a refresh signal having a first state when a refresh operation is in progress and a second state when a refresh operation is not in progress.

3. The RAM of claim 2, wherein the command block is configured to receive the refresh signal and to receive a read command and, in response to receiving the read command, is configured to provide the row signal having the active state at a first time when the refresh signal has the first state and to provide the row signal having the active state at a second time when the refresh signal has the second state, and is configured to provide a read signal having at least a first active state, wherein the at least first active state of the read signal occurs at the set delay after the active state of the row signal, and wherein data is read from at least one memory cell in the opened array in response to the at least first active state of the read signal.

4. The RAM of claim 3, wherein the command block is configured to provide read and write signals each having a series of active states, wherein a first active state of the series occurs at the set delay after the active state of the row signal.

5. The RAM of claim 4, wherein a number of active states of the series is selectable.

6. The RAM of claim 1, wherein the set time is selectable.

7. The RAM of claim 3, wherein the command block comprises:

a command decoder configured to receive a system clock and configured to provide a write indicator signal having an active state in response to the write command and to provide a first a read indicator signal having an active state in response to the read command;

a latency counter configured to provide a delayed write indicator signal having an active state after a first time delay in response the write indicator signal having the active state; and

a signal block configured to provide the row signal having the active state in response to the delayed write indicator signal having the active state and, after a second time delay, configured to provide the write signal having the ate least first active state.

8. The RAM of claim 7, wherein the first time delay and second time delay are each a selectable number of clock cycles of the system clock signal.

9. The RAM of claim 7, wherein the command block further comprises:

an SR flip-flop configured provide a second read indicator signal having an active state at a first output in response to receiving the first read indicator signal having the active state at an S input, and having an R input;

a D flip-flop configured to provide a bar refresh signal having an active state at an output in response to receiving a refresh signal having an inactive state at a D input; and

an AND-gate receiving the bar refresh signal via an inverter at a first input, the clock signal at a second input, and the second read indicator signal at a third input, and providing at an output a third read indicator signal to the signal block and the R input of the SR flip-flop.

10. The RAM of claim 9, wherein the signal block is configured to provide the row signal having the active state in response to the third read indicator signal having an active state and, after the second time delay, to provide the read signal having the at least first active state.

11. The RAM of claim 10, wherein the signal block further comprises:

an OR-gate receiving the third read indicator signal at a first input and the delayed write indicator signal at a second output, and providing a row indicator signal having an active state at an output when third read indicator signal has the active state or the delayed write indicator signal has the active state;

a pulse generator configured to provide the row signal having an active state in response to the row indicator signal having the active state; and

a clock shifter, in response to the row signal having the active state, configured to provide after the second time delay the write signal when the delayed write indicator signal has the active state and the read signal when the delayed write indicator signal has an inactive state.

12. The RAM of claim 1, wherein the command block is further configured to provide the row signal having the active state at the set time in response to receiving a read command, and to provide a read signal having at least a first active state, wherein the first active state of the read signal occurs at the set delay after the active state of the row signal, and wherein data is read from at least one

memory cell in the opened array in response to the first active state of the read signal.

13. The RAM of claim 12, wherein the command block is configured to provide read and write signals each having a series of active states, wherein a first active state of the series occurs at the set delay after the active state of the row signal.

14. The RAM of claim 12, wherein the command block further comprises:

a command decoder configured to receive a system clock and configured to provide a write indicator signal having an active state in response to the write command and to provide a read indicator signal having an active state in response to the read command;

a latency counter configured to provide a pulse signal having an active state after a first time delay in response to either the write indicator signal or the read indicator signal having the active state; and

a signal block configured to receive the write indicator signal and to provide the row signal having the active state in response to the pulse signal having the active state and, after a second time delay, configured to provide the write signal having the at least first active state when the write signal has the active state and to provide the read signal having the at least first active state when the write signal has an inactive state.

15. The RAM of claim 14, wherein the first time delay and second time delay are each a selectable number of clock cycles of the system clock signal.

16. The RAM of claim 14, wherein the signal block further comprises:

a pulse generator configured to provide the row signal having the active state in response to the pulse signal having the active state; and

a clock shifter configured to receive the write indicator signal and, after the second time delay, to provide the write signal having the at least first active

state when the write signal has the active state and to provide the read signal having the at least first active state when the write signal has an inactive state.

17. A method of operating a random access memory, the method comprising:

receiving a write command;

providing a row signal having an active state in response to receiving the write command, wherein the active state occurs at a set time after receipt of the write command;

providing a write signal having at least a first active state, wherein the first active state of the write signal occurs at a set delay after the active state of the row signal.

opening a row of memory cells in an array of memory cells in response to the active state of the row signal; and

writing data to at least one memory cell in the opened row in response to the at least first active state of the write signal.

18. The method of claim 17, further comprising:

providing a refresh signal having a first state when a refresh operation of the array is in progress and a second state when a refresh operation is not in progress;

receiving a read command;

providing the row signal having the active state in response to receiving the read command, wherein the active state occurs at a first time when the refresh signal has the first state and at a second time when the refresh signal has the second state;

providing a read signal having at least a first active state, wherein the first active state occurs at the set delay after the active state of the row signal; and

reading data from at least one memory cell in the opened row in response to the at least first active state of the read signal.

19. The method of claim 18, further comprising:

selecting a number of active states of the write signal and of the read signal.

20. The method of claim 17, further comprising:

receiving a read command;

providing the row signal having the active state at the set time in response to receiving the write command;

providing a reading signal having at least a first active state, wherein the first active state occurs at the set delay after the active state of the row signal;

reading data from at least one memory cell in the opened row in response to the at least first active state of the read signal.

21. A random access memory (RAM) comprising:

means for providing a row signal having an active state in response to receiving a write command, wherein the active state occurs at a set time after receipt of the write command, and for providing a write signal having at least a first active state occurring at a set delay after the active state of the row signal; and

an array of memory cells arranged in a plurality of rows and columns, wherein a selected row is opened for access in response to the active state of the row signal, and wherein data is written to at least one memory cell in the opened row in response to the at least first active state of the write signal.

22. The RAM of claim 22, further comprising:

means for performing autonomous refresh operations of memory cells of the array within the set time and for providing a refresh signal having a first state when a refresh operation is in progress and a second state when a refresh operation is not in progress.

23. The RAM of claim 22, further comprising:

means for providing, in response receiving a read command, the row signal having the active state at a first time when the refresh signal has the first state and for providing the row signal having the active state at a second time when the refresh signal has the second state; and

means for providing a read signal having at least a first active state, wherein the at least first active state occurs at the set delay after the

24. The RAM of claim 21, further comprising:

means for providing the row signal having the active state at the set time in response to a read command; and

means for providing a read signal having at least a first active state, wherein the first active state of the read signal occurs at the set delay after the active state of the row signal, and wherein data is read from at least one memory cell in the opened array in response to the first active state of the read signal.